REMARKS

Claims 1 and 10 have been amended to more clearly recite the "first conductor layer" and its relation to the rest of the claim. Claims 1-15 remain for consideration in the application.

Priority

The examiner states that "...If a parent application has become a patent, the expression 'now Patent No.____' should follow the filing date of the parent application..." At the time of filing the application, the parent application had not yet been issued, nor had the issue fee been paid in the parent, and therefore, the Applicant provided all available information at the time of filing. Applicant has amended the Specification herewith to reflect the subsequent patent issuance information of "Patent No. 6,665,207, issued on December 16, 2003."

Claim Objections

Claims 1-9 were objected to because of alleged informalities in line 7 of claim 1, wherein the examiner states that there is insufficient antecedent basis for "the first conductor plate". Claims 1 and 10 have been amended to more clearly recite the "first conductor layer" and its relation to the rest of the claim.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-2, 4-11 were rejected under 35 U.S.C. § 102(b) as being anticipated by Parekh (U.S. Patent No. 6,140,172). Applicant traverses this rejection, and submits that Parekh does not contain each and every element of the claims and as such the rejection is improper.

Specifically, claims 1 and 10 each recite "a method of fabricating an integrated circuit read only memory (ROM) cell." This is not shown in Parekh. Parekh is directed solely to fabrication of dynamic random access memory (DRAM) cells. In fact, making the connections to a program voltage as recited in claims 1 and 10 clearly defeats the sole purpose of Parekh and would render it unusable as a DRAM.

Further, claim 1 recites "selectively removing a portion of the second conductor layer and the dielectric layer to expose the first conductor layer; and electrically coupling the exposed first conductor to receive a program voltage." This is clearly not present in Parekh which is directed

to DRAM cells. The removal of material to form a bitline plug does not connect a program voltage to the first conductive layer, as the layer to which Parekh connects the bitline plug is electrically isolated from the actual memory cell structure of Parekh. The connection is a bitline plug, and that is all.

Specifically with respect to claim 10, in no part of the Office Action is forming "a plug opening and expose the first conductor layer; and forming a conductive plug in the plug opening to electrically couple the first conductor to receive a program voltage" as is recited in claim 10 discussed. In fact, the bitline plug 160 of Parekh is simply a connection to a bitline, not to a program voltage. Still further, the bitline plug 160 of Parekh is not in contact with the first conductive layer of the cell as is alleged in the Office Action, since the layers of material that the plug 160 contacts are electrically isolated from the actual memory cells. Still further, the memory cells are clearly DRAM cells, and not ROM cells as is recited in the claim.

Applicant respectfully submits that claims 1 and 10 are allowable. Claims 2-9 and 11 depend from and further define one of patentably distinct claims 1 or 10 and are also believed allowable.

Allowable Subject Matter

Applicant thanks the Examiner for the allowance of claims 12-15.

CONCLUSION

Applicant submits that the claims are in condition for allowance, and requests withdrawal of the rejections and the issuance of a Notice of Allowance. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2203.

Respectfully submitted,

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